

REMARKS

The above amendments and following remarks are submitted in response to the Official Action of the Examiner mailed December 13, 2002. Having addressed all objections and grounds of rejection, claims 1-20, being all the pending claims, are now deemed in condition for allowance. Reconsideration to that end is respectfully requested.

The Examiner has objected to the specification as containing a number of informalities. In response thereto, Applicants have amended the specification and abstract as required. These above amendments as supported by Appendix A are deemed to fully address these objections.

Claims 1-3 have been rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,061,766, issued to Lynch et al (hereinafter referred to as "Lynch"). This ground of rejection is respectfully traversed as to amended claims 1-3 for the following reasons.

"It is axiomatic that for prior art to anticipate under §102 it has to meet every element of the claimed invention, and that such a determination is one of fact". *Hybritech Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d 1367, 231 USPQ 81, 90 (Fed. Cir.

1986). Lynch does not "meet every element of the claimed invention".

In making his rejection, the Examiner states:

As per claim 1, Lynch discloses a data processing system having a system bus (i.e., *common memory bus*) and having a processor with a level one cache memory (i.e., CPU 302, *on-board caches 308*) responsively coupled to a level two cache memory (i.e., *cache 306*) which is responsively coupled to a level three cache memory (i.e., *main memory*) [Fig. 3; lines 36-43];

The only mention of a "common memory bus" is at column 1, lines 28-29, which states:

The CPU 102 contains multiple processors which share the main memory via the common memory bus (not shown).....

Thus, this component is admittedly not shown by Lynch. However, to make this limitation even more explicit, claim 1 has been amended to require specific coupling of the "system bus" which cannot be found within Lynch.

Secondly, claim 1 is limited by a "level three cache memory". This element is not found at all in Lynch. Instead, the Examiner disingenuously states:

....which is responsively coupled to a level three cache memory (i.e., *main memory*) [Fig. 3; col. 3, lines 36-43]

Lynch simply does not teach or suggest a "level three cache memory" as is limiting of the claim. None is shown in Fig. 3 as falsely stated by the Examiner. Furthermore, the cited portion of Lynch (i.e., column 3, lines 36-43) mentions a "main memory"

but does not mention or suggest a "level three cache memory" which is limiting of the claimed invention. The Examiner provides no "evidence of inherency" as required by MPEP 2112.

Claim 1 requires "a circuit for SNOOPing said system bus". Because Lynch teaches no "system bus", it cannot have "a circuit for SNOOPing said system bus". Instead, the Examiner cites column 3, line 60. Of Lynch which states:

Reference number 314 is a dedicated pipelined snoop bus which transmits

Therefore, unlike the claimed invention which requires "a circuit for SNOOPing said system bus", Lynch has a "dedicated pipelined snoop bus". Clearly, any finding of the Examiner to the contrary is clearly erroneous.

Further limiting of claim 1 is the "First logic" of element a. This element is simply not found in Lynch's preferred embodiment of Fig. 3. Recognizing this situation, the Examiner cites column 1, lines 40-48 and 53-55, of Lynch. Clearly, this citation discusses a prior art embodiment alleged by Lynch, rather than the preferred embodiment of his disclosed invention. Thus, the Examiner has impermissibly attempted to combine elements from different and mutually exclusive embodiments of Lynch.

Furthermore, even if the citation were not impermissibly combined with elements from a mutually exclusive embodiment, the

citation does not teach or suggest the claimed element which requires "First logic which invalidates a corresponding level one cache memory location in response to either a non-local memory write or write ownership request". Therefore, the rejection of claim 1, and the claims depending therefrom is respectfully traversed for failure of the Lynch reference to "meet every element of the claimed invention" as required by the controlling law.

Claim 2 depends from claim 1 and is further limited by "second logic which inhibits said first logic from invalidating for mode 3 requests without ownership". This structure is not found in Lynch. Instead, the Examiner clearly erroneously cites Lynch Fig. 4 and column 4, lines 19-30. This citation shows no structure for "inhibiting invalidation based upon mode 3 requests without ownership". In fact, Lynch says nothing of "mode 3 requests" (i.e., it has no level three cache memory) and says nothing of "ownership". To the extent that the Examiner has found otherwise, he has based his rejection on clearly erroneous findings of fact. The rejection of claim 2 is respectfully traversed.

In attempting to reject claim 3, the Examiner impermissibly cites the same structure used to show the "second logic". In other words, the Examiner has improperly equated a single element

within Lynch with two different elements of the claimed invention. Thus, the rejection of claim 3 is respectfully traversed.

In rejecting claim 4, the Examiner cites Fig. 4, steps 408-420 to show "fourth logic which "retrieves and records data....". Any fair reading of Lynch reveals that none of these steps either "retrieves" or "records" data. The rejection of claim 4 is respectfully traversed.

The Examiner has rejected claim 6 under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,397,300, issued to Arimilli et al (hereinafter referred to as "Arimilli"). This ground of rejection is respectfully traversed for failure of Armilli to "meet every element of the claimed invention" as required by controlling law.

Claim 1, as amended, is limited by "A level three cache memory responsively coupled to said level two cache memory via said system bus". Arimilli has no level three cache memory.

Furthermore, claim 6 is limited by "A first circuit which invalidates a corresponding portion of said level one cache memory in response to a level one cache memory write hit and a level two cache memory write". Because Armilli does not contain this element, the Examiner paraphrases the claim by stating:

....if hit in upper level cache, cache line in upper level cache invalidated.

Clearly, this is not invalidation requiring a simultaneous "level two cache memory write". Thus, the rejection of claim 6 is respectfully traversed because Arimilli does not "meet every element of the claimed invention" as required by controlling law.

Claims 11 and 16 have been rejected under 35 U.S.C. 102(e) as being anticipated by Arimilli. The Examiner has lumped together his rejection for these two claims even though they have different statutory and procedural bases of patentability. The Examiner is required by law to examine claim 16, and the claims depending therefrom under MPEP 2181, et seq. Thus, the rejection of claim 16 is respectfully traversed as being improperly examined as a matter of law.

Claim 11 is a four step method claim. Armilli does not have step c. In making his rejection, the Examiner states:

second experiencing a level two cache memory hit in
response to said first experiencing step [col. 9, lines
33-34, col. 12, lines 54-56]

This finding is clearly erroneous. The material cited at column 9, lines 33-34 clearly refers to a read access rather than a write access as is limiting of claim 11. Column 12, lines 54-56 does not even refer to the claimed step. Rather the write request is made to both L1 and L2 caches simultaneously (because

the L1 cache is a store-through cache). Column 12, lines 12-13 states:

It also enters a queue 242 to L1 cache, and a queue 244 to the L2 cache.

The rejection of claim 11 is respectfully traversed because Armilli does not "meet all of the claimed elements" as required by controlling law.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lynch in view of U.S. Patent No. 4,891,809, issued to Hazawa. This ground of rejection is respectfully traversed for failure of the Examiner to make a *prima facie* case of obviousness as specified by MPEP 2143. This provision requires the Examiner to show: 1) motivation to make the alleged combination; 2) likelihood of success of the alleged combination; and 3) all claimed elements within the alleged combination.

The Examiner has not even addressed the requirement to show "likelihood of success". The rejection is respectfully traversed.

As to motivation, the Examiner states:

It would have been obvious to one of ordinary skill in the art, having the teachings of Lynch and Hazawa before him at the time the invention was made, to modify the system of Lynch to include invalidating a level one cache memory in response to a level two cache memory generating a parity error because it would have provided a cache memory having a normal error checking mode as taught by Hazawa by the provision of a sequential verification logic circuit for generating

error indicating signals in sequence within the cache memory unit [col. 1, lines 30-37] as taught by Hazawa.

This is precisely the unsupported conclusion attacked by the Court of Appeals for the Federal Circuit stating in part:

Broad conclusory statements regarding the teaching of multiple references, standing alone, are not "evidence". *In re Dembiczak*, 175 F.3d 994, 50 U.S.P.Q. 2d 1614 (Fed. Cir. 1999).

Therefore, the rejection is respectfully traversed for failure to show motivation as well.

In addition, the alleged combination does not have all of the claimed elements. The claim is limited by "Fifth logic....which in response invalidates said corresponding level one cache memory location". There is no showing that the alleged combination performs such invalidation in response to the detected parity error. Thus, the rejection of claim 5 is respectfully traversed for failure of the Examiner to make any of the three showings required by MPEP 2143.

Claims 7-9, 12-14, and 17-19 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli in view of Lynch. Claims 10, 15, and 20 have been rejected under 35 U.S.C. 103a) as being unpatentable over Arimilli. These grounds of rejection are respectfully traversed for failure of the Examiner to make a *prima facie* case of obviousness as specified by MPEP 2143. Again, the Examiner does not even allege "likelihood of

success". Furthermore, the Examiner has not shown evidence of motivation as required by the CAFC, as explained above, but has rather only provided a conclusory statement. Therefore, these rejections are respectfully traversed.

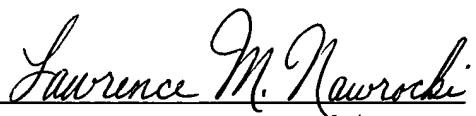
Having thus responded to each objection and ground of rejection, Applicants respectfully request entry of this amendment and allowance of claims 1-20, being the only pending claims.

Respectfully submitted,

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By his attorney,

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